



(11) **EP 2 267 897 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:  
**29.12.2010 Bulletin 2010/52**

(21) Application number: **10175243.4**

(22) Date of filing: **18.02.2003**

(51) Int Cl.:  
**H03K 19/003** (2006.01) **G11C 5/14** (2006.01)  
**G11C 11/4074** (2006.01) **G05F 1/46** (2006.01)  
**G05F 3/24** (2006.01) **G06F 13/40** (2006.01)

(84) Designated Contracting States:  
**DE FR**

(30) Priority: **31.05.2002 JP 2002159696**

(62) Document number(s) of the earlier application(s) in  
accordance with Art. 76 EPC:  
**03003649.5 / 1 369 997**

(71) Applicant: **Fujitsu Semiconductor Limited**  
**Kohoku-ku, Yokohama-shi**  
**Kanagawa 222-0033 (JP)**

(72) Inventor: **Tanishima, Hideaki**  
**Aichi 487-0013 (JP)**

(74) Representative: **Seeger · Seeger · Lindner**  
**Partnerschaft Patentanwälte**  
**Paosostrasse 95**  
**81249 München (DE)**

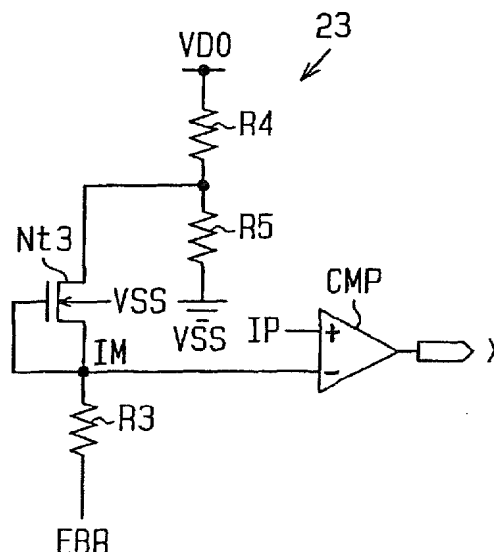
Remarks:

This application was filed on 03-09-2010 as a  
divisional application to the application mentioned  
under INID code 62.

(54) **Input/output buffer**

(57) An input/output buffer that protects a circuit from voltage signals provided from an external device. The input/output buffer includes a reference power generation circuit (16) connected to a high voltage power supply and a low voltage power supply to convert the voltage of an external voltage signal and generate reference power. The reference power generation circuit (16) has a protection circuit (17) including a plurality of MOS transistors (Pt11-Pt15) for decreasing the voltage of the external voltage signal to a predetermined voltage when the input/output buffer is not supplied with the voltage of the high voltage power supply. Each of the MOS transistors has a back gate connected to a predetermined node at which the voltage is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

**Fig.18A**



**EP 2 267 897 A1**

## Description

[0001] The present invention relates to an input/output buffer, an input buffer, and an output buffer.

[0002] Due to the recent progress in multimedia and the popularity of asymmetric digital subscriber line (ADSL) and wireless LAN, the number of households having personal computers (PC) has increased. It is required that the power consumption be reduced in peripheral equipment of a personal computer. Thus, the circuits of the peripheral equipment are miniaturized and operated with low voltage. Such low voltage circuits must be protected when the circuits are not supplied with power or when the low voltage circuits are provided with a voltage signal that is greater than the operational voltage.

[0003] A PC is normally connected to a display, a mouse, a printer, a memory, a modem, or a game device by means of a bus or an input/output port (I/O port).

[0004] A bus is classified as an internal bus or an external bus. The internal bus connects the CPU and the memory. The external bus connects the CPU and an I/O port (e.g., graphic board or SCSI board). Examples of an external bus include, for example, industrial standard architecture (ISA), peripheral component interconnect (PCI), small computer system interface (SCSI), IEEE 1394, universal serial bus (USB), integrated drive electronics (IDE), and AT attachment (ATA).

[0005] The I/O port is an interface connecting the PC and the peripheral equipment and normally includes a port exclusive connector. The I/O port includes a serial port connected to, for example, a mouse and modem, a parallel port connected to a printer, and a game port connected to a game device.

[0006] Fig. 1 is an explanatory diagram illustrating a layout example of connection pins in a game port (joystick port), which is connected to a joystick. A joystick port connector 71, which includes +5 V (volts) power supply terminals, digital input terminals, analog input terminal, and ground terminals, may be connected to joysticks A and B. An example in which the joysticks A and B each have two buttons will now be discussed.

[0007] The +5 power terminals are normally directly connected to a motherboard, and current flows through the +5 power supply terminals to the motherboard. Digital signals (A1, A2, A3, A4 in Fig. 1) are input from the buttons of the joysticks A and B, which are connected to the port. The digital input terminals receive, for example, a signal having a low level (V) when the buttons of the joysticks A and B are pushed and a signal having a high level when the buttons of the joysticks A and B are not pushed.

[0008] The analog input terminals receive an analog signal (AX, AY, BX, BY) that is in accordance with the resistances of the joysticks A and B.

[0009] More specifically, the joystick port includes a one shot multivibrator 72 as shown in Fig. 2, which is connected to an analog input terminal via an input/output buffer 73. A resistor 74 having a resistance of, for exam-

ple, 2.2k $\Omega$  is connected between the analog input terminals and the multivibrator 72. A 0.011 $\mu$ F timing capacitor 75 is connected between the output terminal of the multivibrator 72 and a ground terminal. The joysticks A and B each have a variable resistor 76 (0 to 100k $\Omega$ ). The resistor 76 has a first terminal connected to a +5 power supply terminal and a second terminal connected to the analog input terminal.

[0010] When the analog input terminal is provided with an analog signal from the joysticks A and B, the multivibrator 72 generates an output signal having a high level (5 V). The high output signal charges the capacitor 75. When the voltage of the capacitor 75 reaches 3.3 V, the multivibrator 72 generates a signal at a low level (0 V). When the multivibrator 72 is outputting the high signal, the resistance of the joysticks A and B is proportional to the resistance of the variable resistors 76. In other words, position information of the joysticks A and B may be detected from the resistance of the variable resistor 76.

[0011] Due to the decrease in the operational voltage of the interface (I/O port), the circuits used in peripheral equipment are not operated under the same power supply voltage. Thus, an input/output buffer for the I/O port must be able to accept signals having a voltage that is greater than the operational voltage of the input/output buffer.

[0012] For example, when the power supply voltage of the input/output buffer 73 is 3.3 V, a 5 V voltage signal for operating the joysticks A and B is input to the input terminal of the input/output buffer 73. In this case, the input/output buffer 73 must be able to accept a 5 V voltage signal.

[0013] The following input/output buffers are known to be able to accept signals having a voltage that is greater than the power supply voltage:

- first prior art example, input/output buffer having a tolerant function; and
- second prior art example, input/output buffer having a voltage resistance function at a circuit section to which a voltage signal, which is greater than the operational voltage, is applied in the input/output buffer.

[0014] Fig. 3 is a schematic block diagram of an input/output buffer 81 according to the first prior art example. The input/output buffer 81 includes an input/output circuit 82, an input circuit 83, an output circuit 84, and a tolerant circuit 85.

[0015] The input/output circuit 82 sends a voltage signal EB, which is an external input signal, to the input circuit 83 and the tolerant circuit 85. The tolerant circuit 85 generates a voltage signal BP having a voltage that is in accordance with the input voltage signal EB. The input circuit 83 generates a signal X by adjusting the voltage signal EB (external input signal) to an optimal signal X and outputting the signal X to an internal circuit (not shown).

[0016] The output circuit 84 receives a data signal A

and an output control signal C from the internal circuit. The output circuit 84 generates control signals AP and AN in accordance with an output control signal C and provides the control signals AP and AN to the input/output circuit 82. The input/output circuit 82 generates the voltage signal EB in response to the control signals AP and AN and sends the voltage signal EB to the external equipment.

[0017] The circuits of the input/output buffer 81 will be described in more detail. The output circuit is a generally used circuit and thus will not be discussed.

[0018] Fig. 4 is a circuit diagram of the input/output circuit 82. The input/output circuit 82 includes p-channel MOS transistors (PMOS transistors) Pt1 and Pt2 and n-channel MOS transistors (NMOS transistors) Nt1 and Nt2.

[0019] The transistors Pt1 and Pt2 are connected in series, and the source of the transistor Pt1 is connected to a first high voltage power supply VDE. The gate of the transistor Pt1 receives the control signal AP from the output circuit 84. The drain of the transistor Pt1 is connected to the source of the transistor Pt2. The gate of the transistor Pt2 is connected to a low voltage power supply VSS, and the drain of the transistor Pt2 is connected to the drain of the transistor Nt1.

[0020] The back gates of the transistor Pt1 and the transistor Pt2 are each connected to the output of the tolerant circuit 85 and has substantially the same voltage as the voltage signal BP, which is generated by the tolerant circuit 85.

[0021] The transistors Nt1 and Nt2 are connected in series, and the source of the transistor Nt2 is connected to the low voltage power supply VSS. The drains of the transistors Pt2, Nt1 are connected to each other, and a node N1 between the transistors Pt2 and Nt1 is connected to an input/output terminal 82a of the voltage signal EB. A first high voltage power supply VDE is a power supply for supplying an external circuit that is connected to the input/output buffer 81 with operational voltage and has, for example, a voltage of 3.3 V. The low voltage power supply VSS is the ground (GND).

[0022] The gate of the transistor Nt1 is connected to the first high voltage power supply VDE, and the back gate of the transistor Nt1 is connected to the low voltage power supply VSS. The gate of the transistor Pt2 receives the control signal AN from the output circuit 84, and the back gate of the transistor Nt2 is connected to the low voltage power supply VSS.

[0023] Fig. 5 is a circuit diagram of the tolerant circuit 85. The tolerant circuit 85 includes a resistor R1 and PMOS transistors Pt3 to Pt5.

[0024] The resistor R1, which is an input protection circuit, has one end connected to the node N1 (input/output circuit 82) of the input/output circuit 82 and another end connected to the gate of the transistor Pt3. The resistor R1 decreases the voltage of the voltage signal EB, which is input to the input/output circuit as an external input signal). The voltage signal EB of which voltage has

been decreased (voltage signal EBR) is provided to the gate of the transistor Pt3.

[0025] The source of the transistor Pt3 is connected to the first high voltage power supply VDE, and the drain of the transistor Pt3 is connected to the source of the transistor Pt4. The transistors Pt4 and Pt5 are connected in series and have gates that are connected to the first high voltage power supply VDE. The drain of the transistor Pt5 is connected to a node N2 between the resistor R1 and the transistor Pt3. The drain of the transistor Pt5 is provided with the gate voltage of the transistor Pt3 (voltage signal EBR).

[0026] The back gates of the transistors Pt3 to Pt5 are connected to the back gates of the other transistors and to a node between the transistors Pt3 and Pt4. The tolerant circuit 85 outputs the voltage signal BP, the voltage of which is the same as the voltage at the node between the transistors Pt3 and Pt4.

[0027] Fig. 6 is a circuit diagram of the input circuit 83. The input circuit 83 includes PMOS transistors Pt6 to Pt8 and NMOS transistors Nt3 to Nt7. The drain of the transistor Nt3 is connected to the first high voltage power supply VDE, and the source and gate of the transistor Nt3 are connected to each other. The transistors Nt4 and Nt5 are connected in series, and the gates of the transistors Nt4 and Nt5 are connected to the first high voltage power supply VDE. The source of the transistor Nt5 is connected to the node N2 of the tolerant circuit 85 and receives the gate voltage of the transistor Pt3 (voltage signal EBR). The drain of the transistor Nt4 is connected to the source of the transistor Nt3, and the voltage at node N3 between the transistors Nt4 and Nt3 is supplied to the gates of the transistors Pt7 and Nt6. The back gates of the transistors Nt3 to Nt5 are each connected to the low voltage power supply VSS.

[0028] The source of the transistor Pt6 is connected to the first high voltage power supply VDE, and the gate of the transistor Pt6 is connected to the node N2 of the tolerant circuit 85 to receive the voltage signal EBR. The drain of the transistor Pt6 is connected to the source of the transistor Pt7, and the transistor Pt7 is connected to the transistor Nt6. The source of the transistor Nt6 is connected to the low voltage power supply VSS. The back gates of the transistors Pt6 and Pt7 are connected to the output of the tolerant circuit 85 and have about the same voltage as the voltage signal BP. The back gate of the transistor Nt6 is connected to the low voltage power supply VSS.

[0029] The gates of the transistors Pt8 and Nt7 are connected to the drains of the transistors Pt7 and Nt6. The source of the transistor Pt8 is connected to a second high voltage power supply VDI, and the drain of the transistor Pt8 is connected to the drain of the transistor Nt7. The source of the transistor Nt7 is connected to the low voltage power supply VSS. The second high voltage power supply VDI is a power supply for supplying the internal circuit with operational voltage and has, for example, 1.8V. The back gate of the transistor Pt8 is con-

nected to the second high voltage power supply VDI, and the back gate of the transistor Nt7 is connected to the low voltage power supply VSS. The signal X, which has the drain voltage of the transistors Pt8 and Nt7, is provided to the internal circuit (not shown).

**[0030]** An example in which the voltage signal EB (external input signal) is input to the input/output buffer 81 will now be discussed.

1. Case in which the voltage signal EB is close to the voltage of the low voltage power supply VSS:

In this case, the transistor Pt3 switches on in the tolerant circuit 85. Accordingly, the tolerant circuit 85 outputs the voltage signal BP, the voltage of which is the same as the first high voltage power supply VDE.

In the input circuit 83, the transistor Pt6 switches on and the source of the transistor Pt7 is connected to the first high voltage power supply VDE. In this state, the power supply VDE activates the transistors Nt4 and Nt5, and the transistor Nt3 is inactivated. This inputs the voltage signal EBR to the gates of the transistors, which in turn, activates the transistor Pt7 and inactivates the transistor Nt6. As a result, the gates of the transistors Pt8 and Nt7 are connected to the high voltage power supply VDE. This inactivates the transistor Pt8 and activates the transistor Nt7. Accordingly, the input circuit outputs the signal X, which has the voltage of the low voltage power supply VSS, that is, a low level.

2. Case in which the voltage signal EB is close to the voltage of the high voltage power supply VDE (under the condition that  $EB < VDE$  is satisfied):

In this case, in the tolerant circuit 85, it is difficult for the transistors Pt3 to Pt5 to switch on, and the transistors Pt3 to Pt5 substantially function as a series-connected resistor. Accordingly, the tolerant circuit 85 outputs the voltage signal EBR, or the voltage signal BP that has about the same voltage as the first high voltage power supply VDE.

In the input circuit 83, the transistor Pt6 switches off. In this state, although it is difficult for the transistors Nt3 to Nt5 to switch on since the gate-source voltage is small, a voltage signal having a voltage that is slightly lower than that of the high voltage power supply VDE (e.g., the voltage signal being about 3.1 V when the high voltage power supply VDE has 3.3 V) is input to the gates of the transistors Pt7 and Nt6. In response to the voltage signal, the transistor Pt7 switches on and the transistor Nt6 switches on. As a result, the low voltage power supply VSS is connected to the gates of the transistors Pt8 and

Nt7. This activates the transistor Pt8 and inactivates the transistor Nt7. Accordingly, the input circuit 83 outputs the voltage of the second high voltage power supply VDI, or the signal X at a high level.

3. Case in which the voltage signal EB exceeds the first high voltage power supply VDE:

In this case, in the tolerant circuit 85, the transistor Pt5 switches on since its source voltage (voltage signal EBR) is greater than the gate voltage (high voltage power supply VDE). In this state, the transistor Pt4 switches on in the same manner. Accordingly, the tolerant circuit 85 outputs the voltage signal BP, the voltage of which is about the same as that of the voltage signal EB.

In the input circuit 83, the transistor Pt6 is inactivated. In this state, the transistor Nt4 switches off since its source voltage (voltage signal EBR) is greater than the gate voltage (high voltage power supply VDE). In the same manner, the transistor Nt5 switches off. However, the gate voltage of the transistor Nt3 increases and activates the transistor Nt3. In this state, the gates of the transistors Pt7 and Nt6 are provided with the voltage signal, the voltage of which is decreased from that of the first high voltage power supply VDE by the threshold voltage of the transistor Nt3. In response to the voltage signal, the transistor Pt7 switches off, and the transistor Nt6 switches on. As a result, the gates of the transistors Pt8 and Nt7 are connected to the low voltage power supply VSS. This activates the transistor Pt8 and inactivates the transistor Nt7. Accordingly, the input circuit 83 outputs the voltage of the second high voltage power supply VDI, or the signal X at a high level.

**[0031]** The back gates of the transistors Pt6 and Pt7 have the same voltage as that of the voltage signal (voltage adjusted in accordance with the voltage signal EB). Thus, even if the voltage of the voltage signal EB is greater than that of the first high voltage power supply VDE, the gate voltage becomes greater than the back gate voltage and prevents the generation of a leak current in the transistors Pt6 and Pt7. Accordingly, the input/output buffer 81 adjusts the voltage signal EB to a proper voltage (the operational voltage of the internal circuit) and outputs the voltage signal EB even if an external input signal having the voltage signal EB (e.g., 5 V), which is greater than the operational voltage (3.3 V), is input to the input/output buffer 81.

**[0032]** When the first high voltage power supply VDE does not supply the input/output buffer 81 with power (inactivated state), devices may be damaged and a leakage current may flow in the input/output buffer 81. Nor-

mally, in a personal computer or the like, a power supply circuit is continuously supplied with power. In this state, a voltage signal may be input to the inactivated input/output buffer 81 from an external circuit. In such a case, the application of a voltage greater than the power supply voltage may damage devices or produce leakage current.

**[0033]** More specifically, if the high voltage signal EB is input to the input/output buffer from an external device when the input/output buffer 81 is not supplied with power (high voltage power supply VDE), voltage greater than that of the power supply VDE is applied between the gate and drain of the transistor Pt2 and the gate and source of the transistors Nt1, Pt3, Pt5, Pt6, and Nt5. In such a case, high voltage, which is greater than the operational voltage, is applied to the gate oxidation film of each transistor. This produces short circuits between gates and drains and between gates and sources. Thus, the input/output buffer 81 is not suitable for equipment having a hot plug function.

**[0034]** In the input/output buffer having a voltage resistance function at the predetermined circuit sections, the gate oxidation film that directly receives the high voltage signal must be formed thickly while the gate oxidation films of the other transistors are formed with the normal thickness. This increases the circuit cost and increases the processing time.

**[0035]** To solve the above problem, Japanese Laid-Open Patent Publication No. 2000-29551 uses a buffer protection circuit, which will now be discussed.

**[0036]** Fig. 7 is a circuit diagram of a prior art voltage generator 91, which is a buffer protection circuit. The voltage generator 91 includes PMOS transistors 92 to 94 and NMOS transistors 95 to 97. The source of the transistor 92 and the gate of the transistor 95 are connected to a power supply VDD. The drain of the transistor 95 is connected to the gate of the transistor 92, and the source of the transistor 95 is connected to a power supply VSS (ground). Two diode-connected transistors 96 and 97 are connected in series between the drain of the transistor 92 and a terminal PAD.

**[0037]** When the power supply voltage VDD exists, the voltage generator 91 generates the reference voltage VDD2 having about the same voltage as the power supply voltage VDD. When the power supply voltage VDD does not exist, the voltage generator 91 drops the voltage of the voltage signal input to the terminal PAD by a voltage corresponding to two diodes. The voltage generator 91 adjusts the voltage signal input to the terminal PAD to a proper voltage and generates reference voltage VDD2. This protects circuits from high voltage signals input to the terminal PAD regardless of whether or not the power supply VDD exists.

**[0038]** However, the voltage generator 91 (Fig. 7) has the shortcomings described below.

(1) The back gates of the transistors are connected to the power supply VSS (ground). Thus, when the

power supply VDD does not exist ( $VDD = 0$ ), high voltage is applied between the gate and back gate of each of the transistors 96 and 97. This causes device deterioration. Such a shortcoming also occurs when the transistors 96 and 97 are PMOS transistors.

(2) To sufficiently control the voltage drop in the diode-connected transistors 96 and 97, the transistor 94 configures a DC path between the terminal and the power supply VSS. However, in the DC path, the voltage of the power supply VDD decreases to about the same voltage as the power supply VSS. Further, when the transistor 94 is activated, the reference voltage VDD2 decreases. Thus, the reference voltage VDD2 having the intended voltage level cannot be generated. When an NMOS transistor configures the transistor 94 and the power supply VSS configures the gate input of the transistor 94, the path through which current flows is eliminated. As a result, the high voltage signal input to the terminal PAD cannot be decreased to the proper voltage to generate the reference voltage VDD2.

(3) The forward direction of the diode configured by the transistors 96 and 97 is the direction from node A to the terminal PAD. Thus, when the voltage at node A becomes greater than that at the terminal PAD (e.g., if the voltage of the voltage signal provided to the terminal PAD is the same as the voltage of the power supply voltage (ground)), current flows from the node A to the terminal PAD. This decreases the reference voltage VDD2 and the reference voltage VDD2 cannot be generated with the intended voltage level. If a high voltage signal is input to the terminal PAD when PMOS transistors configure the transistors 96 and 97, the effect of junction temperature increases the resistance of each PMOS transistor. This increases the difference between the voltages applied to each PMOS transistor and damages the device.

**[0039]** It is desirable to provide an input/output buffer, an input buffer, and an output buffer that protect circuits from voltage signals provided by an external device regardless of whether power is being supplied.

**[0040]** According to an embodiment of one aspect of the present invention there is provided an input/output buffer for use with a high voltage power supply and a low voltage power supply and receiving an external voltage signal. The input/output buffer includes a reference power generation circuit connectable to the high voltage power supply and the low voltage power supply for converting the voltage of the external voltage signal and generating reference power. The reference power generation circuit having a protection circuit including a plurality of MOS transistors for decreasing the voltage of the external voltage signal to a predetermined voltage when the input/output buffer receives the external voltage signal and is not supplied with the voltage of the high voltage power

supply. Each of the MOS transistors has a back gate connected to a predetermined node at which the voltage is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

**[0041]** According to an embodiment of another aspect of the present invention there is provided an input/output buffer for receiving an external voltage signal via a resistor and a reference voltage signal. The input/output buffer having an input circuit including an n-channel MOS transistor and a comparator connected to the n-channel MOS transistor. The n-channel MOS transistor includes a source for receiving the external voltage signal via the resistor, a gate connected to the source, and a drain for receiving reference power, the voltage of which is divided by a divisional resistor. The comparator compares the external voltage signal with the reference voltage signal to determine whether the voltage of the external voltage signal is greater than a predetermined threshold voltage from the comparison.

**[0042]** According to an embodiment of another aspect of the present invention there is provided a method for protecting an input/output buffer from a voltage signal that is provided from an external device. The input/output buffer is connected to a high voltage power supply and a low voltage power supply and includes an input/output circuit for transferring data with the external device. The method including decreasing the voltage of the voltage signal to a predetermined voltage with a plurality of MOS transistors, which are connected in series between the high voltage power supply and the low voltage power supply. Each MOS transistor has a back gate to generate reference power when the input/output buffer is not supplied with the voltage of the high voltage power supply. The method further includes supplying the input/output circuit with the reference power, and supplying the back gate of each MOS transistor with voltage that is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

**[0043]** According to an embodiment of another aspect of the present invention there is provided an input buffer for use with a high voltage power supply and a low voltage power supply and for receiving an external voltage signal. The input buffer includes a reference power generation circuit connectable to the high voltage power supply and the low voltage power supply for converting the voltage of the external voltage signal and generating reference power. The reference power generation circuit having a protection circuit including a plurality of MOS transistors for decreasing the voltage of the external voltage signal to a predetermined voltage when the external voltage signal is received and the voltage of the high voltage power supply is not supplied. Each of the MOS transistors has a back gate connected to a predetermined node at which the voltage is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

**[0044]** According to an embodiment of another aspect

of the present invention there is provided an input buffer for receiving an external voltage signal via a resistor and a reference voltage signal. The input buffer has an input circuit including an n-channel MOS transistor and a comparator connected to the n-channel MOS transistor. The n-channel MOS transistor includes a source for receiving the external voltage signal via the resistor, a gate connected to the source, and a drain for receiving reference power, the voltage of which is divided by a divisional resistor. The comparator compares the external voltage signal with the reference voltage signal to determine whether the voltage of the external voltage signal is greater than a predetermined threshold voltage from the comparison.

**[0045]** According to an embodiment of another aspect of the present invention there is provided an output buffer for use with a high voltage power supply and a low voltage power supply and receiving an external voltage signal. The output buffer includes a reference power generation circuit connectable to the high voltage power supply and the low voltage power supply for converting the voltage of the external voltage signal and generating reference power. The reference power generation circuit has a protection circuit including a plurality of MOS transistors for decreasing the voltage of the external voltage signal to a predetermined voltage when the output buffer receives the external voltage signal and is not supplied with the voltage of the high voltage power supply. Each of the MOS transistors has a back gate connected to a predetermined node at which the voltage is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

**[0046]** Other aspects and advantages of the present invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

**[0047]** The invention and preferred objects and advantages thereof, may best be understood by reference to the following description of the certain exemplifying embodiments together with the accompanying drawings in which:

Fig. 1 is an explanatory diagram illustrating connection pins of a joystick port in the prior art;

Fig. 2 is an explanatory diagram illustrating an analog input of a joystick port;

Fig. 3 is a schematic block diagram of a prior art input/output buffer;

Fig. 4 is a circuit diagram illustrating an input/output buffer of Fig. 3;

Fig. 5 is a circuit diagram illustrating a tolerant circuit of the input/output buffer of Fig. 3;

Fig. 6 is a circuit diagram illustrating an input circuit of the input/output buffer of Fig. 3;

Fig. 7 is a circuit diagram of a prior art voltage generator;

Fig. 8 is a schematic block diagram illustrating an

input/output buffer according to a first embodiment of the present invention;

Fig. 9 is a circuit diagram illustrating an input/output circuit of the input/output buffer of Fig. 8;

Fig. 10 is a circuit diagram illustrating a tolerant circuit of the input/output buffer of Fig. 8;

Fig. 11 is a circuit diagram illustrating an input circuit of the input/output buffer of Fig. 8;

Fig. 12 is a circuit diagram illustrating a power generation circuit of the input/output buffer of Fig. 8;

Fig. 13 is an explanatory diagram illustrating a protection circuit of the power generation circuit of Fig. 12;

Fig. 14 is an explanatory diagram illustrating an operation example of the power generation circuit of Fig. 12;

Fig. 15 is an explanatory diagram illustrating a further example of a protection circuit;

Figs. 16A and 16B are explanatory diagrams illustrating further examples of a protection circuit;

Fig. 17 is a circuit diagram illustrating an input/output circuit according to a second embodiment of the present invention;

Figs. 18A and 18B are circuit diagrams illustrating input circuits of the second embodiment;

Fig. 19 is a schematic block diagram illustrating an input buffer according to a third embodiment of the present invention;

Fig. 20 is a schematic block diagram illustrating an output buffer of the third embodiment;

Figs. 21A to 21C are explanatory diagrams illustrating a pull-up input buffer according to a fourth embodiment of the present invention;

Figs. 22A and 22B are explanatory diagrams illustrating the input buffer of Figs. 21A to 21C provided with a fail-safe function;

Figs. 23A and 23B are explanatory diagrams illustrating the pull-up input buffer of the fourth embodiment;

Figs. 24A and 24B are explanatory diagrams illustrating the input buffer of Figs. 23A and 23B provided with a fail-safe function; and

Fig. 25A and 25B are explanatory diagrams of the input/output circuit of the first embodiment provided with a fail-safe function.

**[0048]** In the drawings, like numerals are used for like elements throughout.

**[0049]** Fig. 8 is a schematic block diagram of an input/output buffer 11 according to a first embodiment of the present invention. The input/output buffer 11 includes an input/output circuit 12, an input circuit 13, an output circuit 14, a tolerant circuit 15, and a power generation circuit (reference power generation circuit) 16.

**[0050]** The input/output circuit 12 provides a voltage signal EB, which is an external input signal EB, to the input circuit 13, the tolerant circuit 15, and the power generation circuit 16. In accordance with the voltage of the

voltage signal EB, the power generation circuit 16 generates operational power (reference power) VDO for the input/output buffer 11. The power generation circuit 16 provides the reference power VDO to the input/output circuit 12, the input circuit 13, and the tolerant circuit 15. The tolerant circuit 15 generates a voltage signal BP, the voltage of which corresponds with the input voltage signal EB. In accordance with the reference power VDO, the input circuit 13 adjusts the voltage signal EB to a proper voltage to generate a signal X and outputs the signal X to an internal circuit (not shown).

**[0051]** When the output circuit 14 receives a data signal A and an output control signal C from the internal circuit, the output circuit 14 generates control signals AP and AN in accordance with an output control signal C. The control signals AP and AN are provided to the input/output circuit 12. In response to the control signals AP and AN, the input/output circuit 12 generates the voltage signal EB and outputs the voltage signal EB (output signal).

**[0052]** The configuration of each circuit in the input/output buffer 11 will now be discussed in detail. The output circuit 14 is a widely used circuit and thus will not be discussed.

Fig. 9 is a circuit diagram of the input/output circuit 12. The input/output circuit 12 includes PMOS transistors Pt1 and Pt2 and NMOS transistors Nt1 and Nt2. In the input/output circuit 12, the source of the transistor Pt1 and the gate of the transistor Nt1 are supplied with the reference power VDO. The remaining parts of the input/output circuit 12 are the same as those of the input/output circuit 82 illustrated in Fig. 4.

Fig. 10 is a circuit diagram of the tolerant circuit 15. The tolerant circuit 15 includes a resistor R1, which is a protection resistor, and PMOS transistors Pt3 to Pt5. In the tolerant circuit 15, the source of the transistor Pt3 and the gates of the transistors Pt4 and Pt5 are supplied with the reference power supply VDO. The remaining parts of the tolerant circuit 15 are the same as those of the tolerant circuit 85 illustrated in Fig. 5.

Fig. 11 is a circuit diagram of the input circuit 13. The input circuit 13 includes PMOS transistors Pt6 to Pt8 and NMOS transistors Nt3 to Nt7. In the input circuit 13, the source of the transistor Pt6, the drain of the transistor Nt3, and the gates of the transistors Nt4 and Nt5 are supplied with the reference power VDO. The remaining parts of the input circuit 13 are the same as those of the input circuit 83 illustrated in Fig. 6.

Fig. 12 is a circuit diagram of the power generation circuit 16. The power generation circuit 16 includes PMOS transistors Pt9 to Pt15, NMOS transistors Nt8 to Nt12, and a resistor R2.

**[0053]** The gates of the transistors Nt8 and Pt9 and

the source of the transistor Pt10 is connected to a high voltage power supply VDE (e.g., 3.3 V). The source of the transistor Nt8 is connected to a low voltage power supply VSS (ground), and the drain of the transistor Nt8 is connected to the source of the transistor Pt9 and the gate of the transistor Pt10. The back gate of the transistor Nt8 is connected to the low voltage power supply VSS. The back gates of the transistors Pt9 and Pt10 are connected to the output of the tolerant circuit 15 and have about the same voltage as the voltage signal BP.

**[0054]** The transistors Pt11 to Pt14 are connected in series to the drain of the transistor Pt9. The transistor Pt15 is connected to the transistor Pt14 so that the transistors Pt11 to Pt14 are connected in a reverse direction. The voltage signal EB is input to the drain of the transistor Pt15 via the resistor R2, which is used for electrostatic discharge (ESD) protection.

**[0055]** The transistors Nt9 to Nt12 (voltage-maintaining circuit 18) are connected in series. The gate of each of the transistors Nt9 to Nt12 is connected to the associated drain, and the back gate of each of the transistors Nt9 to Nt12 is connected to the low voltage power supply VSS. The source of the transistor Nt12 is connected to the low voltage power supply VSS. The drain of the transistor Nt9 is connected to the source of the transistor Pt10 and the source of the transistor Pt11. The power generation circuit 16 outputs the reference power VDO, the voltage of which is the same as the voltage at node N4.

**[0056]** In the power generation circuit 16, the transistors Pt11 to Pt15, which are diode-connected, function as a protection circuit 17.

**[0057]** Fig. 13 is an explanatory diagram illustrating the transistor configuration in the protection circuit 17. As shown in Fig. 13, the transistors Pt11 to Pt15 are PMOS transistors formed on, for example, a p-type silicon substrate. The back gate of each of the transistors Pt11 to Pt14 is connected to the associated drain, and the back gate of the transistor Pt15 is connected to the source of the transistor Pt15.

**[0058]** The transistors Pt11 to Pt14 receive the reference power VDO in the forward direction (PN). The transistor Pt15 receives the reference power VDO in the reverse direction. That is, the transistors Pt11 to Pt15 are diode-connected to receive the reference power VDO in the manner of PN-PN-PN-PN-NP.

**[0059]** The operation of the input/output buffer 11 of the first embodiment will now be discussed with reference to Fig. 14. Fig. 14 is an explanatory diagram illustrating an operation example of the power generation circuit 16.

**[0060]** A case in which the input/output buffer 11 is supplied with power (high voltage power supply VDE = 3.3 V) will first be discussed. In this case, in the power generation circuit 16, the transistor Nt8 switches on and connects the gate of the transistor Pt10 to the low voltage power supply VSS. This activates the transistor Pt10. In this state, referring to Fig. 14, the power generation circuit 16 generates the reference power VDO, the voltage of

which is the same as the high voltage power supply VDE, regardless of the voltage of the voltage signal (external input signal) EB. Even when the voltage signal EB, the voltage (e.g., 6 V) of which is greater than the high voltage power supply VDE, is input, the transistors Nt11 to Nt15 decreases the voltage of the voltage signal EB to the voltage of the high voltage power supply VDE (3.3 V). Thus, the reference power VDO is output at about 3.3 V.

**[0061]** A case in which the input/output buffer 11 is not supplied with power (i.e., the high voltage power supply VDE being substantially 0 V) will now be discussed.

**[0062]** In this case, the transistor Nt8 switches off and the transistor Pt9 switches on in the power generation circuit 16. In this state, the transistor Pt10 switches off and the power generation circuit 16 generates the reference power VDO, the voltage of which is in accordance with the voltage signal EB, as shown in Fig. 14.

**[0063]** More specifically, when the input voltage signal EB, has a voltage that is substantially the same as the low voltage power supply VSS, the voltage of the reference power VDO becomes the same as that of the low voltage power supply VSS (0 V). When the input voltage signal EB has a voltage that is substantially the same as the high voltage power supply VSS (about 3.3 V), the power generation circuit 16 generates the reference power VDO (in Fig. 14, 2.07 V), the voltage of which is obtained by decreasing the voltage of the voltage signal EB with the transistors Pt11 to Pt15.

**[0064]** When the input voltage signal EB has a voltage (e.g., 6 V) that is greater than that of the high voltage power supply VDE, the power generation circuit 16 generates the reference power VDO (in Fig. 14, 3.62 V), the voltage of which is obtained by decreasing the voltage of the voltage signal EB with the transistors Pt11 to Pt15.

**[0065]** In this manner, the power generation circuit 16 generates the reference power VDO at about 3 V even if the voltage signal EB is input when the power generation circuit 16 is not supplied with power (high voltage power supply VDE).

**[0066]** A plurality (four in the first embodiment) of transistors Nt9 to Nt12 are connected between the node N4 and the low voltage power supply VSS (refer to Fig. 12). Thus, the leakage current flowing through the transistors Nt9 to Nt12 is small. In this case, the gate voltages at the transistors Nt9 to Nt12 are respectively 3.3 V, 2.16 V, 1.24 V, and 0.52 V, and the leakage current in the path of the transistors Nt9 to Nt12 is reduced to several tens of nanoamperes.

**[0067]** Since the transistor Pt15 is connected to the transistors Pt11 to Pt14 in the reverse direction (NP) and is reverse biased, reverse leakage current does not flow through the path of the transistors Pt11 to Pt15. The gates of the transistors Pt11 to Pt15 are connected to a lower voltage side (source side) when the voltage signal EB decreases voltage. Thus, the transistors Pt11 to Pt15 stably function. In addition to suppressing device deterioration, which is caused by an increase in the resistance component, and voltage fluctuation of the reference pow-



er VDO, the intended reference power VDO is accurately generated. Further, the power generation circuit 16 has the ESD protection resistor R2. Thus, voltage fluctuation is suppressed even when the voltage of the voltage signal EB changes drastically.

[0068] The reference power VDO generated by the power generation circuit 16 is supplied to the input/output circuit 12, the input circuit 13, and the output circuit 14. Thus, regardless of whether the high voltage power supply VDE is supplied, damage to devices and the occurrence of a leakage current is prevented in the input/output buffer 11 regardless of the voltage of the voltage signal EB.

[0069] In the power generation circuit 16 of the first embodiment, the protection circuit 17 may be configured by NMOS transistors Nt13 to Nt17 as shown in Fig. 15. More specifically, the transistor Nt13 receives the reference power supply VDO in the reverse direction (NP). The other transistors Nt14 to Nt17 are connected in a direction that is reversed from the connection direction of the transistor Nt13. That is, the transistors Nt13 to Nt17 are diode-connected to receive the reference voltage VDO in the manner of NP-PN-PN-PN-PN. In this case, the transistor Nt13 stops reverse current leakage.

[0070] The gates of the transistors Nt13 to Nt17 are each connected to the higher voltage side (i.e., drain side) when the voltage is decreased. Thus, the transistors Nt13 to Nt17 are stably operated, fluctuation of the reference power VDO caused by an increase in the resistance component is suppressed, and the reference power VDO is accurately generated with the intended voltage.

[0071] The NMOS transistor protection circuit is more useful than the PMOS transistor protection circuit when laid out on an n-type silicon substrate. That is, when PMOS transistors (transistors Pt11 to Pt15) are laid out on an n-type silicon substrate, a triple well transistor configuration becomes necessary. As the layout area increases, the number of reticles and the number of processing operations increase. This increases costs. Accordingly, it is preferred that the protection circuit 17 be configured by PMOS transistors (transistors Pt11 to Pt15) when using a p-type silicon substrate and that the protection circuit 17 be configured by NMOS transistors (transistors Nt13 to Nt17) when using an n-type silicon substrate.

[0072] The protection circuit 17 may further be configured as shown in Figs. 16A and 16B. In Fig. 16A, the voltages at the back gates of the PMOS transistors Pt11 to Pt15 are each generated from the divisional voltage of the source voltage and the low voltage power supply VSS. The transistors Pt11 to Pt15 are diode-connected to receive the reference power VDO in the manner of NP-NP-NP-NP-NP.

[0073] In Fig. 16B, the back gate voltages of the NMOS transistors Nt13 to Nt17 are each generated from the divisional voltage of the drain voltage and the low voltage power supply VSS. Each transistor Nt13 to Nt17 are diode-connected to receive the reference power VDO in

the manner of PN-PN-PN-PN-PN. In the protection circuits of Figs. 16A and 16B, damage to the device and the occurrence of leakage current caused by the low back gate voltage is prevented.

[0074] The input/output buffer 11 of the first embodiment has the advantages described below.

(1) The power generation circuit 16 of the input/output buffer 11 converts the voltage signal EB, which is input from an external device, to a proper voltage corresponding to the high voltage power supply VDE and generates the reference power VDO. The power generation circuit 16 includes diode-connected transistors Pt11 to Pt15 (protection circuit 17). Further, the back gates of the transistors Pt11 to Pt15 are connected to a node at which the voltage is one other than that of the high voltage power supply VDE and the low voltage power supply VSS. Thus, regardless of whether the high voltage power supply VDE is being supplied, when the voltage signal EB is input, high voltage is prevented from being applied between the gate and back gate of each of the transistors Pt11 to Pt15, and deterioration and damage to the transistor is prevented.

(2) Among the transistors Pt11 to Pt15, the transistors Pt11 to Pt14 are diode-connected to receive the reference power VDO in the forward bias direction (forward direction), and the transistor Pt15 is diode-connected to receive the reference power VDO in the reverse bias direction (reverse direction). Thus, when the reference power VDO is generated, reverse leakage current is not produced and the reference power VDO is maintained at the intended voltage.

(3) The gate of each of the transistors Pt11 to Pt15 is connected to the associated source. When the input voltage signal EB has a voltage that is greater than the voltage of the high voltage power supply VDE and the voltage signal EB causes a decrease in voltage, the source voltage is less than the drain voltage. Thus, the increase in the resistance of the transistors Pt11 to Pt15 prevents voltage fluctuation of the reference power VDO.

(4) The power generation circuit 16 includes a voltage-maintaining circuit 18, which is configured by transistors Nt9 to Nt12. The gate of the transistor Nt9 is connected to the reference power VDO, and the gates of the transistors Nt10 to Nt12 are connected to the high voltage side terminal (drain). Thus, the leakage current that flows through the transistors Nt9 to Nt12 is minimized.

[0075] Fig. 17 is a circuit diagram illustrating an input/output circuit 22 of an input/output buffer 11A according to a second embodiment of the present invention. The input/output buffer 11A of the second embodiment is used as a game port (joystick port) to which a joystick is connected. The input/output buffer 11A is configured by

partially modifying the input/output circuit 12 and input circuit 13 of the input/output buffer 11 in the first embodiment.

**[0076]** The input/output circuit 22 includes two NMOS transistors Nt1 and Nt2 and is provided with an open drain output function. This is because the input/output buffer 11A, which is used as a joystick port, detects position information of the joystick during a period in which the input/output buffer 11A is pulled-up to a power supply of +5 V and the input/output circuit 22 does not require an output having a high level.

**[0077]** Fig. 18A is a circuit diagram illustrating an input circuit 23 of the input/output buffer 11A. The input circuit 23 includes an NMOS transistor Nt3, resistors R3 to R5, a comparator CMP, and a reference circuit 23a. As shown in Fig. 18A, a voltage signal EBR is input to the source of the transistor Nt3 via the resistor R3. Voltage generated by dividing the reference power VDO with the resistors R4 and R5 is input to the drain of the transistor Nt3. The gate and source of the transistor Nt3 are connected to each other. The voltage at a node IM between the source of the transistor Nt3 and the resistor R3 is input to an inverting input terminal of the comparator CMP. A reference voltage signal IP from a reference circuit 23a, which is shown in Fig. 18B, is input to a non-inverting terminal of the comparator CMP. The comparator CMP compares the voltage at the node IM with the voltage of the reference voltage signal IP and generates a signal X at a low level or a high level in accordance with the comparison.

**[0078]** The reference circuit 23a includes resistors R6 to R8, inverter circuits INV1 and INV2, and transfer gates TG1, TG2. Each of the transfer gates TG1 and TG2 includes a PMOS transistor and an NMOS transistor. High voltage side divisional voltage generated from power supply VDE by resistors R6 to R8 is input to the input terminal of the transfer gate TG1. Low voltage side divisional voltage is input to the input terminal of the transfer gate TG2.

**[0079]** The PMOS transistor gate of the transfer gate TG1 and the NMOS transistor gate of the transfer gate TG2 are connected to each other, and the signal X is input to each gate from the comparator CMP via an inverter circuit INV1. Further, the signal X is input to the NMOS transistor gate of the transfer gate TG1 and the PMOS transistor gate of the transfer gate TG2 via the inverter circuits INV1 and INV2.

**[0080]** The transfer gates TG1, TG2 are activated and inactivated in a complementary manner in accordance with the signal X in the reference circuit 23a. The reference circuit 23a generates the reference voltage signal IP having reference voltage REFH when the transfer gate TG1 switches on and generates the reference voltage signal IP having reference voltage REFL when the transfer gate TG2 is activated.

**[0081]** The operation of the input/output buffer 11A, which includes the input circuit 23, will now be discussed. Normally, in an input/output buffer used as the joystick

port, a threshold voltage for recognizing an input as a high level (threshold voltage VIL) and a threshold voltage for recognizing an input as a low level (threshold voltage VIL) are both set at about 3.0 V (power supply voltage (high voltage power supply VDE = 3.3 V) - 0.3 V). That is, in the input/output buffer of the joystick port, the voltage difference between the source and gate of the transistor functioning in accordance with the threshold voltage is about 0.3 V and small. Thus, the operation of the transistor may be instable.

**[0082]** In the input circuit 23 of the second embodiment, the voltage signal EBR is input to the source of the transistor NT3. Thus, the voltage at node IM may be increased to the threshold voltage (about 3.0 V) in accordance with the voltage level of the voltage signal EB (external input signal). In this state, voltage generated by dividing the reference power VDO with the resistors R4 and R5 is input to the drain of the transistor Nt3. This prevents the voltage at the node IM from exceeding a predetermined value.

**[0083]** The reference circuit 23a generates the reference voltage signal IP having the reference voltage REFH (e.g., 3.1 V) at a timing in which the signal X shifts from a low level to a high level. Further, the reference circuit 23a generates the reference voltage signal IP having the reference voltage REFL (e.g., 3.1 V) at a timing in which the signal X shifts from a high level to a low level. That is, the reference circuit 23a, which functions as a Schmitt trigger circuit, stabilizes the output of the comparator CMP.

**[0084]** Accordingly, the input/output buffer 11A of the second embodiment operates stably even when the threshold voltage of an input is high (e.g., 3.0 V) and is especially useful for a joystick port that detects the position information of the joystick.

**[0085]** Fig. 19 is a schematic block diagram of an input buffer 31 according to a third embodiment of the present invention. Fig. 20 is a schematic block diagram of an output buffer 41. In the third embodiment, the input/output buffer 11 (refer to Fig. 8) of the first embodiment is used to configure either the input buffer or the output buffer.

**[0086]** That is, as shown in Fig. 19, the output circuit 14 is deleted from the input/output buffer 11 of the first embodiment. When using the input buffer 31 as a joystick port, the input/output circuit 22 (Fig. 17) and the input circuit 23 (Fig. 18) of the second embodiment may be employed in lieu of the input/output circuit 12 and the input circuit 13. Referring to Fig. 20, in the output buffer 41, the input circuit 13 is eliminated from the input/output buffer 11 of the first embodiment.

**[0087]** An input buffer according to a fourth embodiment of the present invention will now be discussed with reference to Figs. 21A to 24B. In the fourth embodiment, to reduce power consumption, the input buffer includes a pull-up resistor for fixing the voltage signal EB (external input signal) at a high level or a pull-down resistor for fixing the voltage signal EB at a low level.

**[0088]** An input buffer 51 incorporating a pull-up resis-

tor will now be discussed. As shown in Fig. 21A, a control signal PC for electrically disconnecting the input buffer 51 from a pull-up resistor is normally input when testing the input buffer 51. More specifically, as shown in Fig. 21B, an input terminal of the voltage signal EB in the input buffer 51 is connected to one end of an input protection resistor R9. The other end of the resistor R9 is connected to a high voltage power supply VDE via a pull-up resistor R10 and a PMOS transistor Pt21 (switch device). The control signal PC is input to the gate of the transistor Pt21. The gate of the transistor Pt21 is connected to a low voltage power supply VSS (ground) via a pull-down resistor R11, which stabilizes the input level of the control signal PC.

**[0089]** Normally, the control signal PC activates the transistor Pt21 and connects the power supply VDE to the pull-up resistor R10 in the input buffer 51. When conducting a test, the control signal PC inactivates the transistor Pt21 and disconnects the power supply VDE from the pull-up resistor R10. Thus, leakage current does not flow through the pull-up resistor R10 when conducting a test, and the testing of an internal circuit of the input buffer is accurately conducted.

**[0090]** When the input buffer 51 enters a fail-safe mode in a state in which the power supply VDE has 0 V, the voltage signal EB has 5 V, and the control signal has 0 V, as shown in Fig. 21C, a voltage difference of 5 V is produced between the source and drain and drain and gate of the transistor Pt21. Accordingly, there is a need to prevent the transistor Pt21 from being damaged in the fail-safe mode.

**[0091]** Figs. 22A and 22B are explanatory diagrams illustrating an input buffer 51a that is suitable for the fail-safe mode. As shown in Fig. 22A, the control signal PC is input to the gate of the transistor Pt21 via an inverter circuit 52 and a NAND circuit 53 in the input buffer 51A. The source of the transistor Pt21 receives the reference power VDO (refer to Fig. 12).

**[0092]** In the input buffer 51a, a signal having a high level is input to the gate of the transistor Pt21 (referred to as P-Gate in Fig. 22B) in the fail-safe mode (i.e., when the high voltage power supply VDE has 0 V). More specifically, if the control signal PC is input at a low level (0 V) when the power supply VDE has 0 V, a signal having a high level is input to the gate of the transistor Pt21. Further, if the control signal PC is input at a high level (3.3 V) when the power supply VDE has 0 V, a signal having a high level is input to the gate of the transistor Pt21, as shown in Fig. 22B. In this state, the transistor Pt21 is inactivated and thus not damaged.

**[0093]** An input buffer incorporating a pull-down resistor will now be discussed. Referring to Fig. 23A, in an input buffer 61 including a pull-down resistor, an input terminal of the voltage signal EB is connected to one end of an input protection resistor R12. The other end of the resistor R12 is connected to a low voltage power supply VSS via a pull-down resistor R13 and an NMOS transistor Nt21 (switch device). The control signal PC is input to

the gate of the transistor Nt21 via an inverter circuit 62. The gate of the transistor Nt21 is connected to a low voltage power supply VSS via a pull-down resistor R14 for stabilizing the input level of the control signal PC.

**[0094]** When the input buffer 61 enters the fail-safe mode, referring to Fig. 23B, a voltage difference of 5 V is produced between the source and drain, the drain and gate, and the drain and back gate of the transistor Nt21. Accordingly, there is a need to prevent the transistor Nt21 from being damaged in the fail-safe mode.

**[0095]** Figs. 24A and 24B are explanatory diagrams of an input buffer 61a that is suitable for the fail-safe mode. As shown in Fig. 24A, in the input buffer 61a, the control signal PC is input to the gate of the transistor Nt21 via an inverter circuit 63, a NAND circuit 64, and an inverter circuit 62. The source of the transistor Nt21 is connected to the selector circuit 65. The selector circuit 65 controls the source voltage of the transistor Nt21 at the voltage of the low voltage power supply VSS or the voltage signal BP in accordance with whether or not power VDE is supplied.

**[0096]** In the input buffer 61a, a signal having a low level is input to the gate of the transistor Nt21 (referred to as N-Gate in Fig. 24B) in the fail-safe mode (i.e., when the high voltage power supply VDE has 0 V). More specifically, if the control signal PC is input at a low level (0 V) when the power supply VDE has 0 V, a signal having a low level is input to the gate of the transistor Nt21. Further, if the control signal PC is input at a high level (3.3 V) when the power supply VDE has 0 V, a signal having a low level is input to the gate of the transistor Nt21. In this state, the transistor Nt21 is inactivated and thus not damaged.

**[0097]** In the fourth embodiment, the devices of the input buffers 51a, 61a, which include a pull-up resistor or a pull-down resistor, are prevented from being damaged when the input buffers 51a, 61a enter the fail-safe mode.

**[0098]** It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without. Particularly, it should be understood that the present invention may be embodied in the following forms.

**[0099]** Although the first embodiment employs five transistors Pt, any number of transistors may be used, for example, three, four, six, or at least five.

**[0100]** In the first embodiment, the MOS transistors (protection circuit) that decrease the voltage of the voltage signal EB may include p-channel MOS transistors and n-channel MOS transistors.

**[0101]** In the first embodiment, the transistor that undergoes reverse bias due to the reference power VDO is not limited to the transistor Pt15 and may be another transistor, such as the transistor Pt13 or the transistor Pt14. In the protection circuit 17 of Fig. 15, the transistor that undergoes reverse bias due to the reference power VDO is not limited to the transistor Nt13 and may be another transistor, such as one of the transistors Nt14 to

Nt17. That is, the transistor that is in the reverse direction relative to the reference power VDO and undergoes reverse bias due to the reference power VDO is required only to be arranged at a position where it can stop a reverse current leakage.

[0102] In the first embodiment, the number of the n-channel MOS transistors in the voltage-maintaining circuit 18 is not limited to four and may be any number, for example, three, five, or at least two.

[0103] The input/output circuit 12 (Fig. 9) of the first embodiment may be replaced by an input/output circuit 12a that is illustrated in Figs. 25A and 25B and suitable to a fail-safe mode. In the input/output circuit 12a of Figs. 25A and 25B, the gate of the transistor Pt1 is connected to a selector circuit 12b. The selector circuit 12b normally provides a control signal AP (high level or low level), which is received from the output circuit 14 (Fig. 8), to the gate of the transistor Pt1. When entering the fail-safe mode, the selector circuit 12b supplies the reference power VDO to the gate of the transistor Pt1. The gate of the transistor Pt2 is connected to a selector circuit 12c. The selector circuit 12c normally connects the gate of the transistor Pt2 to the low voltage power supply VSS. During the fail-safe mode, the selector circuit 12c supplies the reference power VDO to the gate of the transistor Pt2.

[0104] Thus, in the input/output circuit 12a, devices are prevented from being damaged during the fail-safe mode. This protects the input/output circuit 12a.

[0105] The present examples and embodiments are to be considered as illustrative and not restrictive.

#### Claims

1. An input/output buffer for receiving an external voltage signal via a resistor and a reference voltage signal, the input/output buffer being **characterized by:**

an input circuit (23) including an n-channel MOS transistor (Nt3) and a comparator (CMP) connected to the n-channel MOS transistor, the n-channel MOS transistor including:

a source for receiving the external voltage signal via the resistor;  
a gate connected to the source; and  
a drain for receiving reference power, the voltage of which is divided by a divisional resistor;

wherein the comparator compares the external voltage signal with the reference voltage signal to determine whether the voltage of the external voltage signal is greater than a predetermined threshold voltage from the comparison.

2. The input/output buffer according to claim 1, **characterized in that** the input circuit includes a reference circuit (23a) connected to the comparator and is provided with a Schmitt trigger function that varies the threshold voltage in accordance with the output of the comparator.

3. The input/output buffer according to claim 1, **characterized in that** the input/output buffer is for use with a high voltage power supply and a low voltage power supply, the input/output buffer further comprising:

a reference power generation circuit (16) connectable to the high voltage power supply and the low voltage power supply for converting the voltage of the external voltage signal and generating the reference power, wherein the reference power generation circuit has a protection circuit (17) including a plurality of MOS transistors (Pt11-Pt15) for decreasing the voltage of the external voltage signal to a predetermined voltage when the input/output buffer receives the external voltage signal and is not supplied with the voltage of the high voltage power supply, each of the MOS transistors having a back gate connected to a predetermined node at which the voltage is less than the voltage of the high voltage power supply and greater than the voltage of the low voltage power supply.

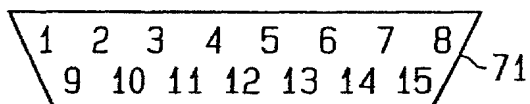
4. An input buffer for receiving an external voltage signal via a resistor and a reference voltage signal, the input buffer being **characterized by:**

an input circuit (23) including an n-channel MOS transistor (Nt3) and a comparator (CMP) connected to the n-channel MOS transistor, the n-channel MOS transistor including:

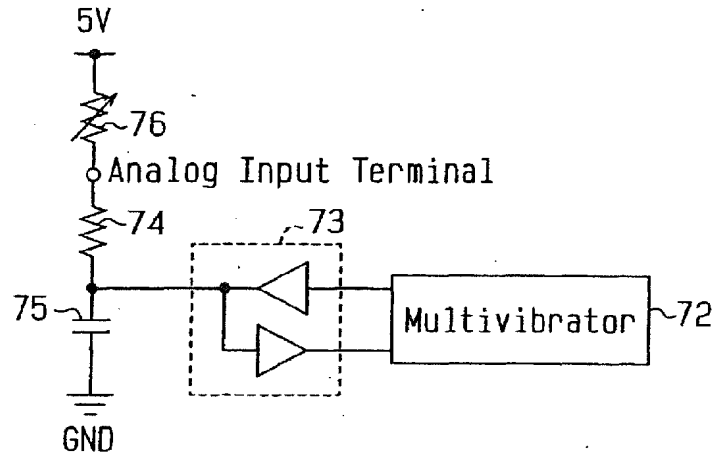
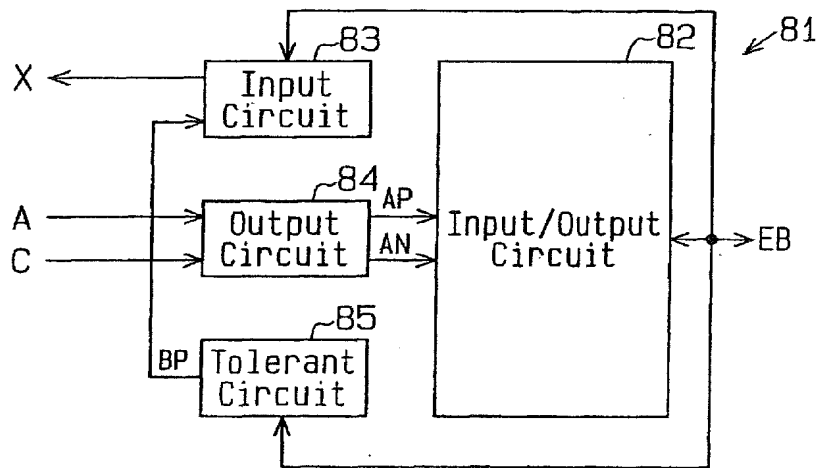
a source for receiving the external voltage signal via the resistor;  
a gate connected to the source; and  
a drain for receiving reference power, the voltage of which is divided by a divisional resistor;

wherein the comparator compares the external voltage signal with the reference voltage signal to determine whether the voltage of the external voltage signal is greater than a predetermined threshold voltage from the comparison.

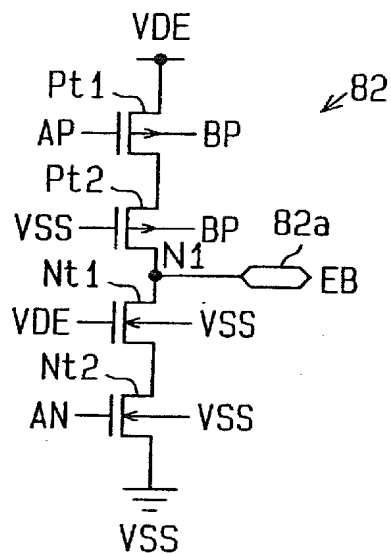
**Fig.1**



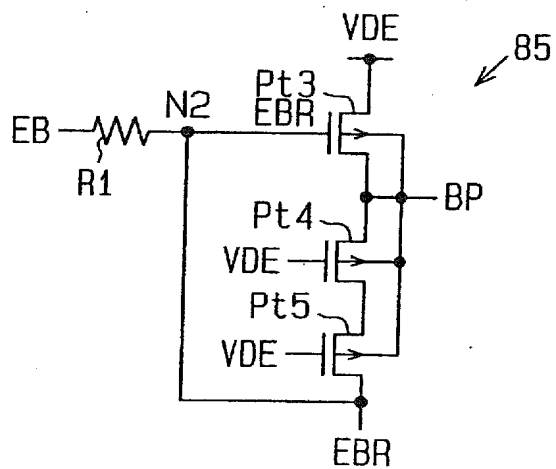
- 1, 8, 9, 15 : +5V Power Supply Terminal
- 4, 5, 12 : Ground Terminal
- 2, 7, 10, 14 : Digital Input (A1, A2, B1, B2) Terminal
- 3, 6, 11, 13 : Analog Input (AX, AY, BX, BY) Terminal

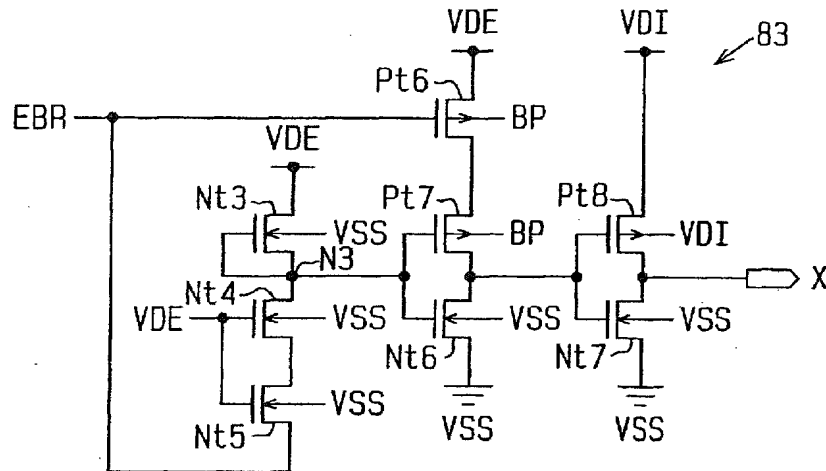
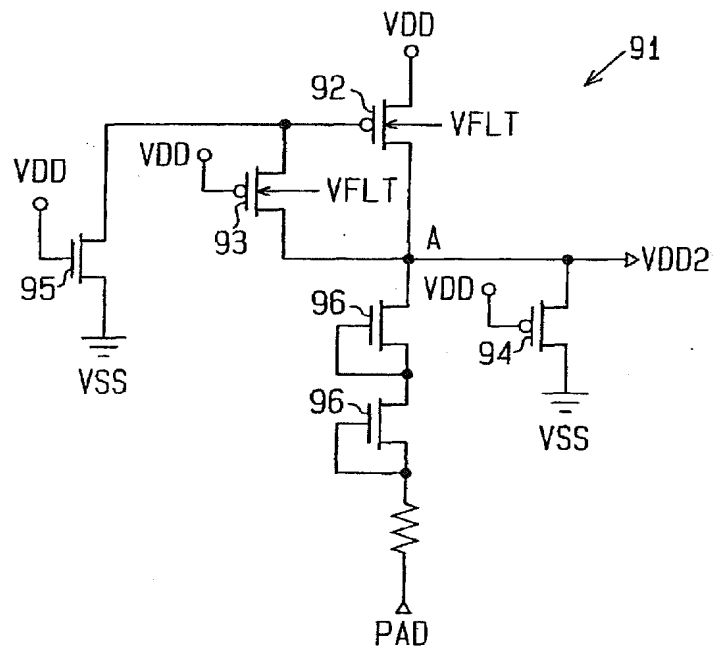
**Fig.2****Fig.3**

**Fig. 4**



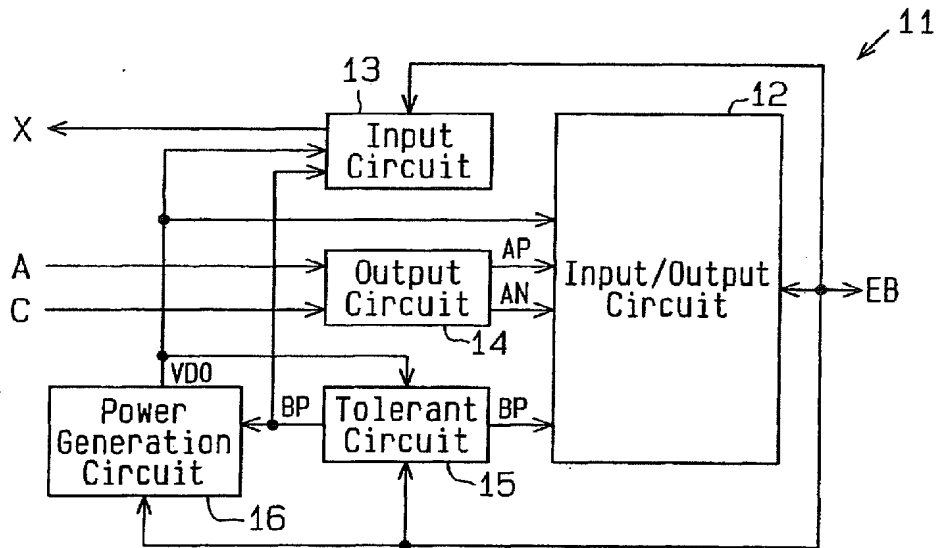
**Fig. 5**



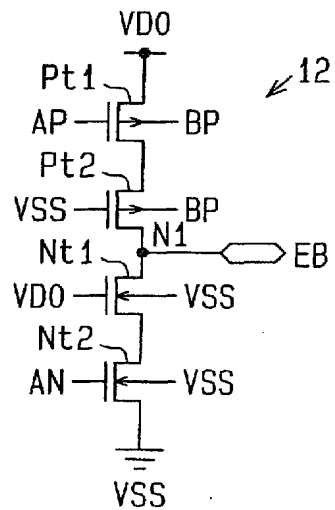
**Fig. 6****Fig. 7**



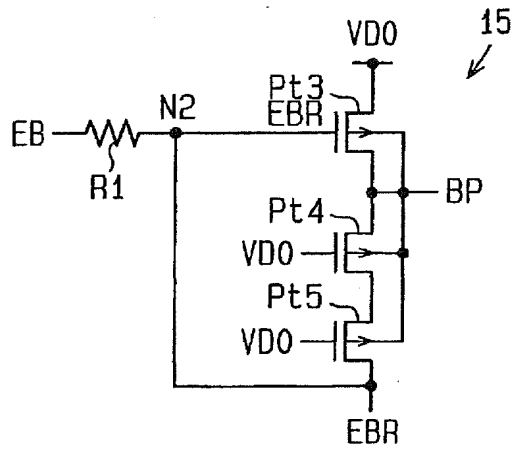
**Fig.8**



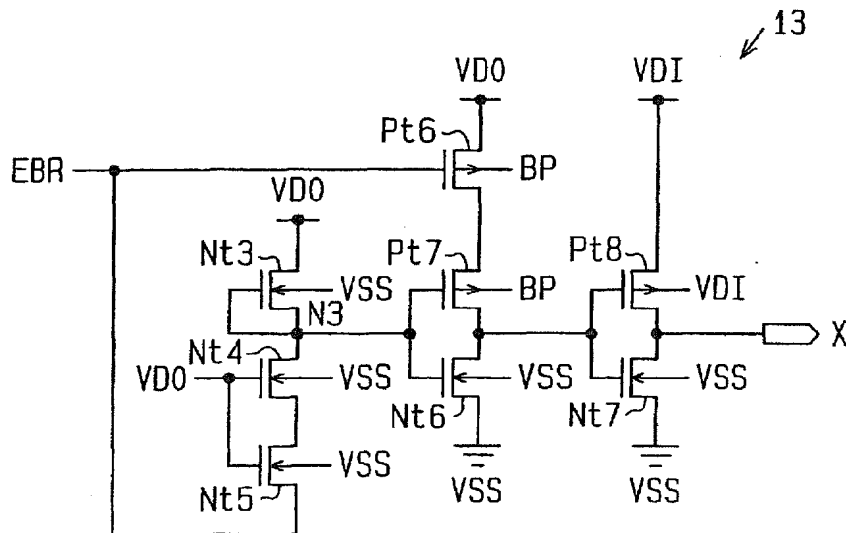
**Fig.9**



**Fig.10**



**Fig.11**





**Fig.14**

Gate for Transistor	VDE=ON			VDE=OFF		
	EB=VSS	EB=VDE	EB=6V	EB=VSS	EB=VDE	EB=6V
Gate of Pt15	2.48V	3.30V	5.59V	0V	3.17V	5.66V
Gate of Pt14	2.17V		5.06V		2.96V	5.19V
Gate of Pt13	2.93V		4.52V		2.74V	4.73V
Gate of Pt12	3.08V		3.84V		2.25V	4.09V
Gate of Pt11	3.30V		3.30V		2.07V	3.62V
VD0	3.30V		3.30V		2.07V	3.62V

**Fig.15**

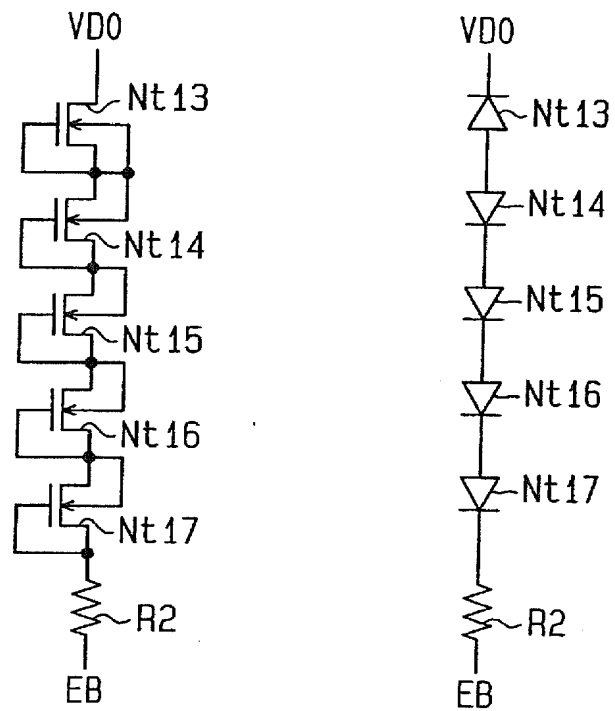


Fig.16B

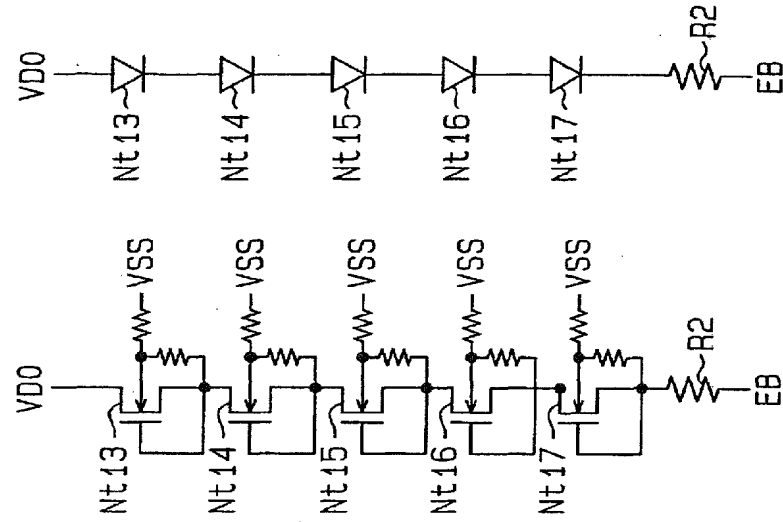
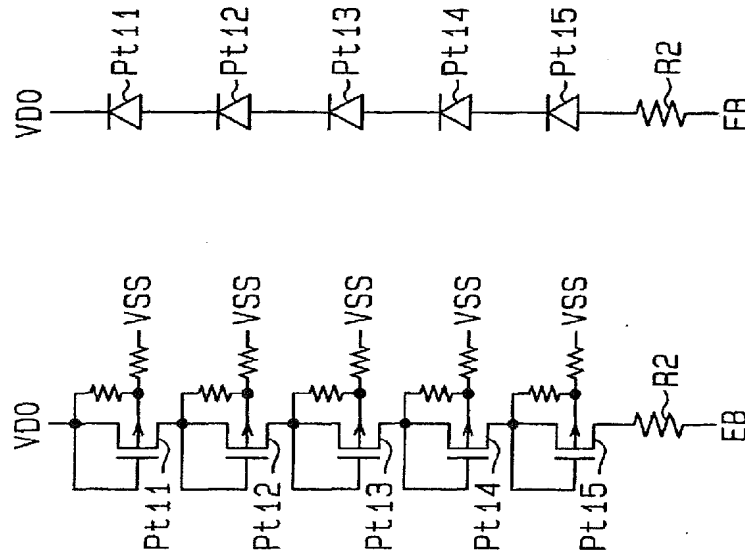
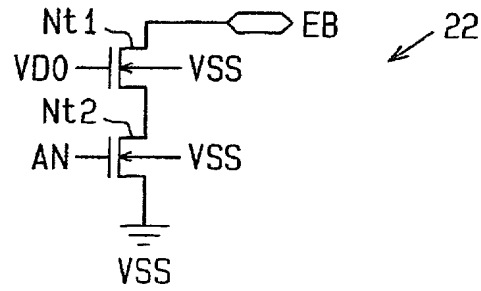


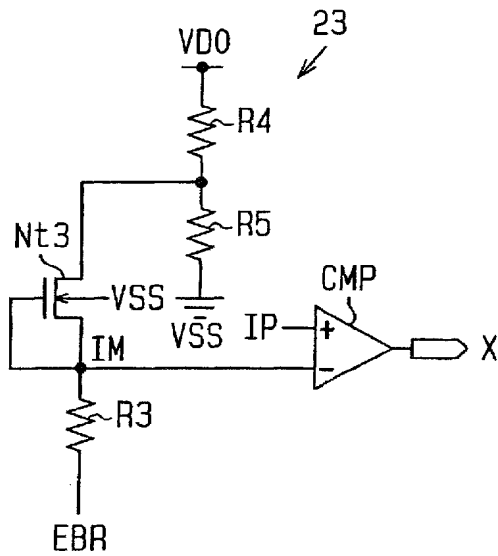
Fig.16A



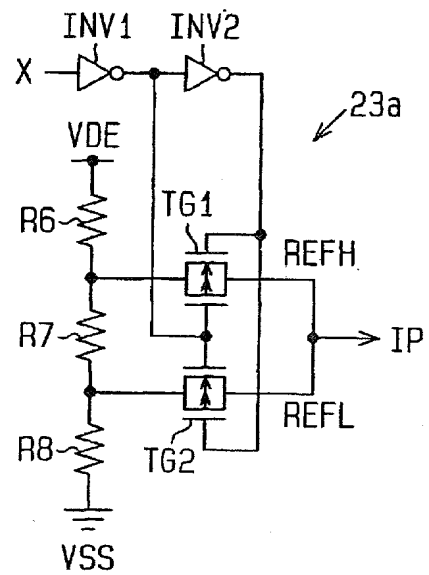
**Fig.17**



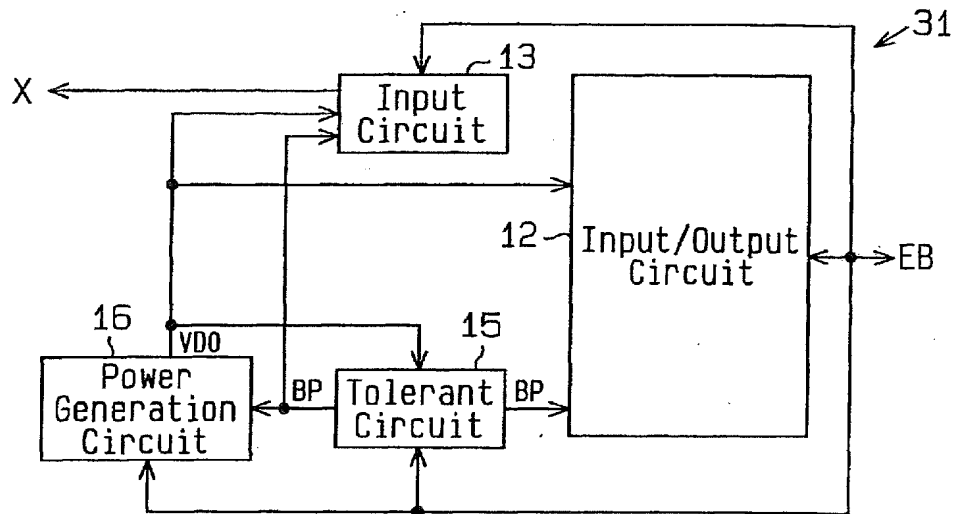
**Fig.18A**



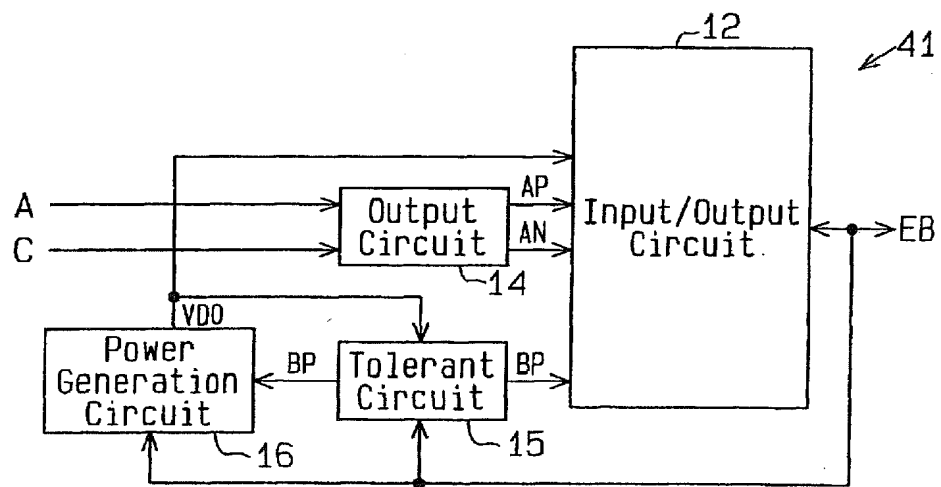
**Fig.18B**



**Fig.19**

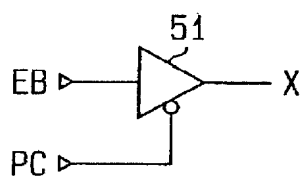


**Fig.20**

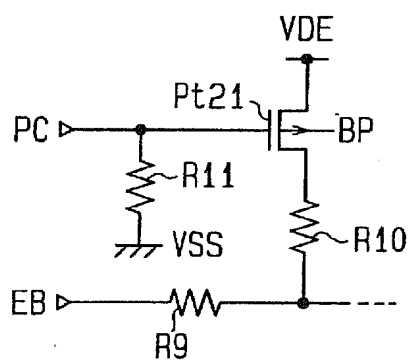




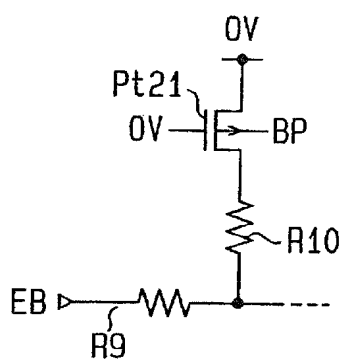
**Fig.21A**

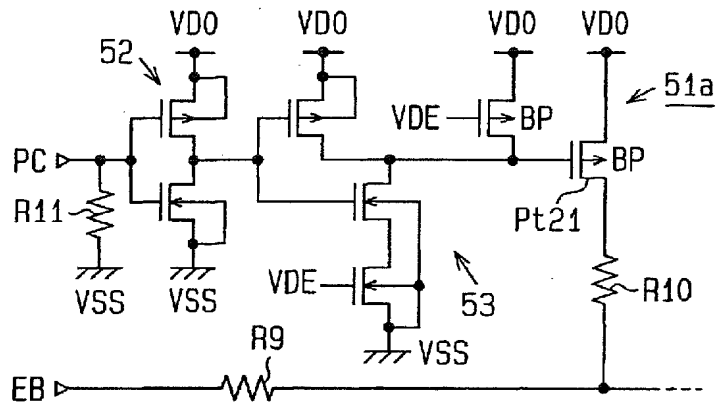


**Fig.21B**



**Fig.21C**



**Fig. 22A****Fig. 22B**

VDE	PC	P-Gate	
1 (3.3 V)	0	L	Normal
1 (3.3 V)	1	H	Test
0 (0 V)	0	H	Fail-Safe
0 (0 V)	1 (0)	H	Fail-Safe

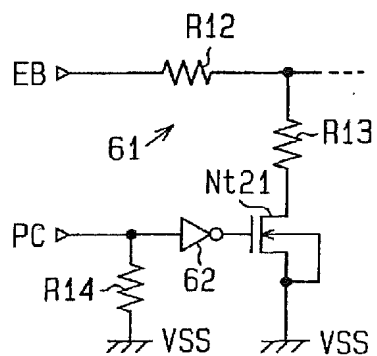
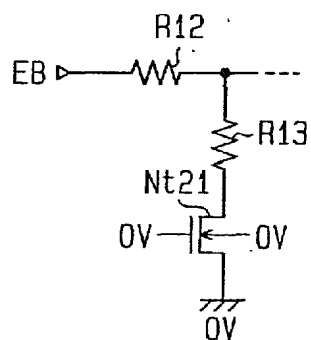
**Fig. 23A****Fig. 23B**

Fig.24A

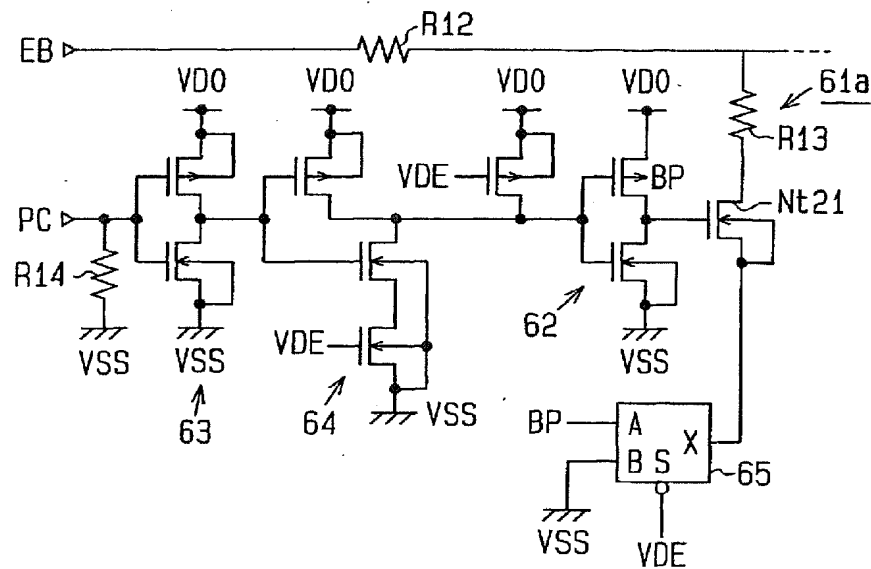
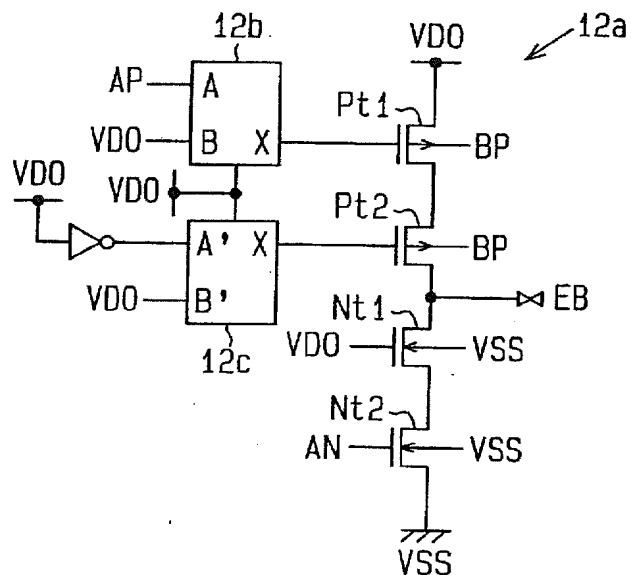


Fig.24B

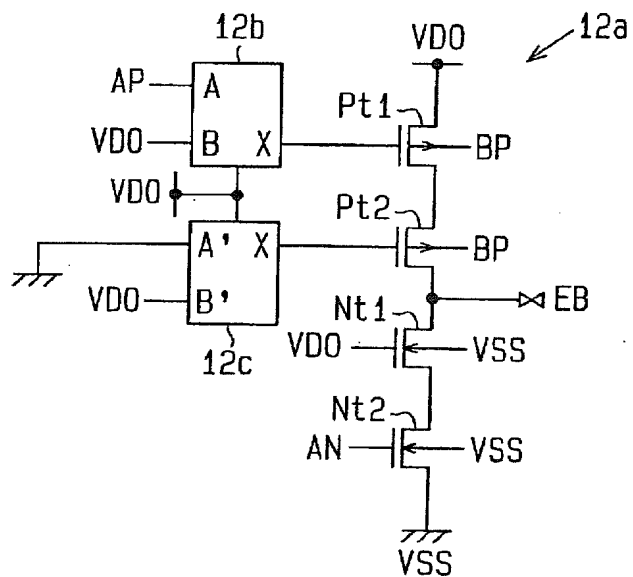
VDE	PC	N-Gate	
1 (3.3 V)	0	H	Normal
1 (3.3 V)	1	L	Test
0 (0 V)	0	L	Fail-Safe
0 (0 V)	1 (0)	L	Fail-Safe

A	B	S	X
BP	VSS	1 (3.3 V)	VSS
		0 (0 V)	BP

**Fig. 25A**



**Fig. 25B**





## EUROPEAN SEARCH REPORT

Application Number  
EP 10 17 5243

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	US 5 304 865 A (SCHOOFS FRANCISCUS A C M) 19 April 1994 (1994-04-19) * figure 1 *	1-4	INV. H03K19/003 G11C5/14 G11C11/4074 G05F1/46 G05F3/24 G06F13/40
A	US 6 084 462 A (BARKER RICHARD J) 4 July 2000 (2000-07-04) * figure 5 *	1-4	
A	US 4 460 985 A (HOFFMAN CHARLES R) 17 July 1984 (1984-07-17) * figure 5 *	1-4	
			TECHNICAL FIELDS SEARCHED (IPC)
			G11C G05F G06F
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 8 November 2010	Examiner Santos, Paulo
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons &amp; : member of the same patent family, corresponding document</p>			

1  
EPO FORM 1503 02.92 (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 10 17 5243

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on  
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

08-11-2010

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
US 5304865	A	19-04-1994	DE	69309337 D1		07-05-1997
			DE	69309337 T2		23-10-1997
			JP	5312851 A		26-11-1993
-----						
US 6084462	A	04-07-2000	DE	69832954 T2		07-09-2006
			EP	0931248 A1		28-07-1999
			WO	9908082 A1		18-02-1999
			JP	2001502435 T		20-02-2001
-----						
US 4460985	A	17-07-1984	DE	3379996 D1		06-07-1989
			EP	0087006 A2		31-08-1983
			JP	1770075 C		30-06-1993
			JP	4047398 B		03-08-1992
			JP	58143492 A		26-08-1983
-----						

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

**REFERENCES CITED IN THE DESCRIPTION**

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

**Patent documents cited in the description**

- JP 2000029551 A [0035]